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DEVELOPMENT OF THE BRAZILIAN FPGA CORRELATOR

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ABSTRACT

The design is for an complex cross-correlator for 6 antennas with 3-level quantization and 5MHz sample rate, including an Walsh function generator and delay lines. This will be integrated in a 400k gate FPGA. The input is the sine and cosine signals from 6 antennas, coming from the digitizer. The output is 15 complex correlations and 6 total-power measurements, which are read by the computer each 104 ms. The digitizer has 3-level window comparators for each antenna, with adjustable threshold levels.

Key-words: correlator, FPGA

INTRODUCTION

A correlator system has to analyze a great quantity of data in real time. Up to recently, this task was left to special-purpose integrated circuits. However, with advances on field-programmable gate arrays (FPGA), it has become possible to implement a correlator in one or more FPGAs (Parsons, 2008). The main advantages are that the FPGA is easily found for purchase, relatively cheap, and can be reprogrammed to increase bandwidth, include polarization, improve the precision of the delay tracking, etc.

Parsons (2008) describes a correlator architecture capable of obtaining the correlations as a function of frequency. In the "FX correlator", a Fourier transform (F) is done for each antenna, in real time, before the correlations (X) are done.

Equivalently, in the "XF correlator", the correlations (X) are made before their Fourier transform (F) are done. However, this method does not apply as well when the number of antennas is large, due to the great increase in simultaneous Fourier transforms to be done.

On the other hand, the system built by Ramesh (2006), with custom correlator chips, does not separate the correlations in frequency. Given the complexity and cost of implementing the real-time Fast Fourier Transform in FPGA, we choose to sacrifice the spectral output at this stage, and implement this simpler system in a single FPGA.

THE CORRELATOR SYSTEM

In the BDA, the 70 MHz I.F. signal from each antenna is split by a hybrid microwave component into sine and cosine signals, which are mixed into baseband signals. These form the inputs to the correlator.

The digitizer

The task of the digitizer is analog-to-digital conversion. It is possible to minimize the computing power of the correlator design by using as few levels as possible, and accepting the increase in digitizing noise. While two levels are enough for solar observation, our three-level design has advantages for weaker sources.

As seen on Figure 1, the baseband signal is fed to two high speed comparators, which together define the three digitizer levels: negative, zero and positive. The digital-to-analog converters supply the reference levels that are adjusted periodically to maintain the optimal balance between the levels. The op-amps buffer and invert the positive-only output of the converters. The total-power information is derived by considering the current reference level and measuring the residual imbalance between the levels.

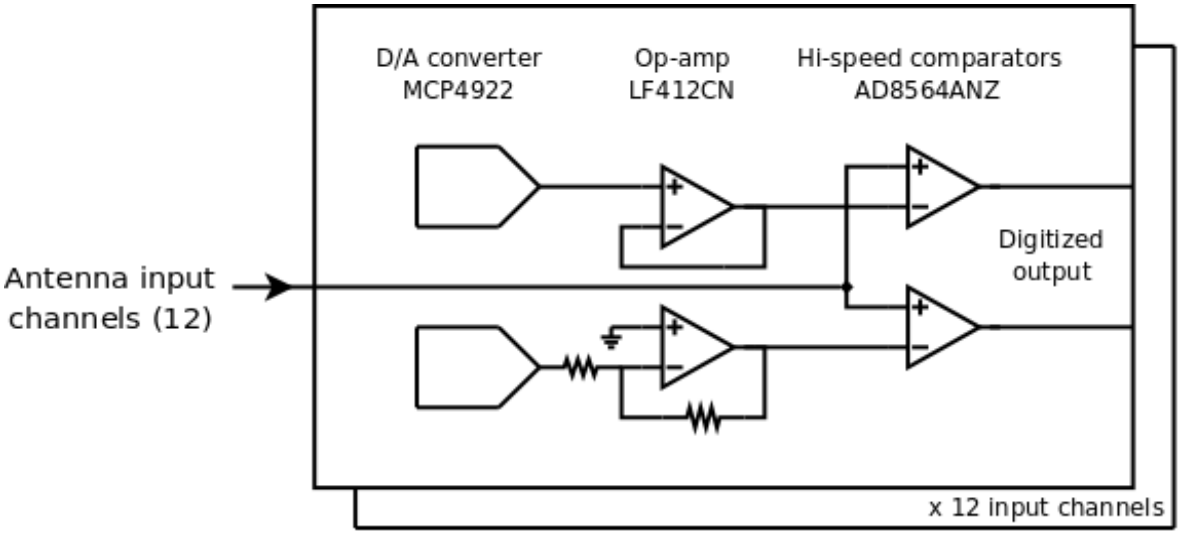

Fig. 1 – Simplified design for a three-level digitizer with automatic level adjustment.

A first batch of prototype digitizer boards were manufactured and are currently undergoing testing.

The FPGA

A commercial FPGA board was acquired from AVNET (DS-KIT-3SLC400) which has a XC3S400 Spartan-3 FPGA, several I/O ports and USB communication. The digitizer connects to the I/O ports while the USB port interfaces to the acquisition computer.

The FPGA was programmed in the Verilog language, implementing a complex correlator circuit based on Ramesh (2006), as shown in Figure 2. One full 3-level complex correlator circuit occupied 72 FPGA slices, or 2% of our 3500-slice FPGA. Six antennas means (6*5)/2=15 correlations, which gives 15*72=1080 slices, well within budget. The Walsh function generator and delay lines (Ramesh, 2006) will also be implemented within the same FPGA.

The design was successfully verified with synthetic data.

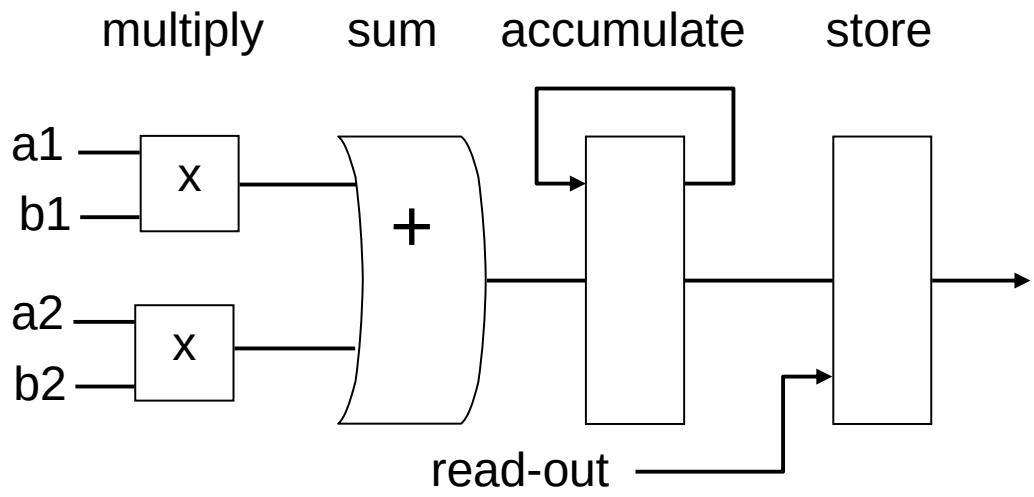

Fig. 2 – Design of a correlator cell. The inputs are the cosine and sine signals from a pair of antennas.

The data acquisition software

In contrast to the current refresh rate of around 50 seconds, we expect to be able to refresh the display at the full rate of 100 ms. This is due to the new correlator design, which continuously outputs data, and the increased speed of new PCs, which gives no chance of data loss.

CONCLUSION

FPGA technology has evolved to the point of replacing custom integrated circuits in highly parallel real-time applications. This results in lowering costs, as these components are available commercially. Given the simple circuit of Ramesh (2006) and the small bandwidths as in the BDA, even a small and cheap ($200) FPGA board is found to be sufficient for 6 antennas.

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